

REMARKS

The Final Office Action dated November 30, 2005, has been received and reviewed.

Claims 1-22 are currently pending and under consideration in the above-referenced application. Each of claims 1-22 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections under 35 U.S.C. § 102

Claims 1-8 and 18-22 stand rejected under 35 U.S.C. § 102.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Shimada

Claims 1-6 stand rejected under 35 U.S.C. § 102(e) for reciting subject matter which is purportedly anticipated by that described in U.S. Patent 6,365,963 to Shimada (hereinafter “Shimada”).

After careful review of the cited art, it is respectfully submitted that Shimada does not anticipate each and every element of independent claim 1 or of any of claims 2-6 depending therefrom.

Shimada describes a “stacked-chip semiconductor device including a rigid insulator board [101] having a first wiring pattern [103] formed on a top surface thereof and an opening [102] formed therein, a base insulator film [110] having a top surface bonded onto a bottom surface of the rigid insulator board [101], the top surface of the base insulator film [110] mounting thereon a second wiring pattern [111] electrically connected to the first wiring pattern [103], a first semiconductor chip [11] mounted on the top surface of the base insulator film [110] and received in the opening [102], the first semiconductor chip [11] having chip electrodes [21] electrically connected to the second wiring pattern [111], and second chip [12] mounted on the rigid

insulator board [101] overlying the opening [102] and chip electrodes [22] connected to the first wiring pattern [103], the first wiring pattern including external electrode pads [106].” Col. 2, lines 19-33; *see also* FIG. 6.

Notably, the back side of the first semiconductor chip 11 is located above an upper surface of the rigid insulator board 101.

Independent claim 1 is directed to a method for assembling a multichip semiconductor device package. The method of independent claim 1 includes, among other things, positioning at least one first-level semiconductor device within a receptacle of a substrate of an interposer, a backside of the at least one first-level semiconductor device being substantially coplanar with a lower surface of the substrate or located within a plane that extends through the substrate. In addition, as amended, independent claim 1 recites “...electrically connecting the at least one first-level semiconductor device to . . . conductors on the upper surface of the substrate by first-level conductive members that are at least partially carried by the second-level semiconductor device...”

As the back side of the first semiconductor chip 11 is located above an upper surface of the rigid insulator board 101 of the assembly disclosed in Shimada, Shimada does not expressly or inherently describe a method that includes positioning at least one first-level semiconductor device in such a way that a backside thereof is substantially coplanar with a lower surface of the substrate of an interposer or is located within a plane that extends through the substrate.

In addition, Shimada lacks any express or inherent description of electrically connecting the at least one first-level semiconductor device to conductors on the upper surface of the substrate by first-level conductive members that are at least partially carried by a second-level semiconductor device. Instead, the description of Shimada is limited to electrically connecting the first semiconductor chip 11 to the second wiring pattern 111 of the base insulator film 110. It is, therefore, respectfully submitted that Shimada does not expressly or inherently describe each and every element of independent claim 1 and, as such, that, under 35 U.S.C. § 102(e), the subject matter recited in independent claim 1 is allowable over the subject matter described in Shimada

Claims 2-6 are each allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Claim 5 is additionally allowable because Shimada neither expressly nor inherently describes forming or positioning intermediate conductive elements between the first semiconductor chip 11 and corresponding conductors of the rigid insulator board 101. Rather, the description of Shimada is limited to positioning solder balls between bond pads of the first semiconductor chip 11 and corresponding portions of the second wiring pattern 111 of the base insulator film 110.

Urushima

Claims 1, 7, and 8 have been rejected under 35 U.S.C. § 102(e) for being drawn to subject matter which is allegedly anticipated by the subject matter described in U.S. Patent 6,791,195 to Urushima (hereinafter “Urushima”).

Urushima describes an assembly that may be formed by positioning a first-level semiconductor device 3d in a hole 51 formed through an interposer 48, positioning two second-level semiconductor devices 3c and 3e over the first-level semiconductor device 3d and portions of an upper surface on the interposer 48, electronically connecting the first-level semiconductor device 3d to the second-level semiconductor devices 3c and 3e, and electrically connecting the second-level semiconductor devices to conductors on the upper surface of the interposer 48. *See*, col. 20, lines 5-56; Fig. 11A.

The method of independent claim 1 includes “...positioning at least one first-level semiconductor device within the receptacle, a backside of the at least one first-level semiconductor device being substantially coplanar with the lower surface of the substrate or located within a plane which extends through the substrate...”

Urushima does not expressly or inherently describe positioning the first-level semiconductor device 3d such that a backside thereof is substantially coplanar with the lower surface of the interposer 48 or located within a plane which extends through the interposer 48. As Fig. 11A clearly depicts, the backside of the first-level semiconductor device 3d is located in a plane below the lower surface of the interposer 48. In fact, roughly one third of the thickness of

the first-level semiconductor device 3d is located outside of the plane in which the lower surface of the interposer 48 is located.

It has been asserted that "...at least one first-level device (3d) within the receptacle, where the backside is substantially or coplanar with the lower surface of the substrate...the deviation in planarity between the bottom surface of the interposer and the chip is quite small, and hence they are "substantially" coplanar..." Office Action, page 4. The term "substantially," when used in conjunction with the term "coplanar," does not mean that a backside and a third of the thickness of a semiconductor device may be located outside of a plane within which the lower surface of an interposer substrate is located. Rather, one of ordinary skill in the art would readily understand that the term "substantially," as used in independent claim 1, encompasses minor positioning and alignment errors that may occur during the manufacturing process, leaving the backside of the first-level semiconductor device not exactly but "substantially" coplanar with the lower surface of the substrate. Thus, one of ordinary skill in the art would readily understand that the phrase "substantially coplanar" does not apply to the method depicted in Fig. 11A of Urushima, where the backside of the first-level semiconductor device 3d is located in a plane below the lower surface of the interposer 48 substrate.

As such, it is respectfully submitted that Urushima does not expressly or inherently describe each and every element of independent claim 1, as would be required to maintain the 35 U.S.C. § 102(e) rejection of independent claim 1.

Among other reasons, claims 7 and 8 each depend directly and indirectly, respectively, from allowable claim 1 and, as such, are both allowable.

Washida

Claims 18-21 are rejected under 35 U.S.C. § 102(b) for being directed to subject matter which is purportedly anticipated by that described in U.S. Patent 5,949,135 to Washida et al. (hereinafter "Washida").

Washida describes semiconductor device assembly methods in which a first semiconductor device 760, is positioned within a hole 701a, of a substrate 700. The

semiconductor device 760 is electrically connected to a second semiconductor device 750, which is positioned over the hole 701a.

It has been asserted that “since the chip (second-level semiconductor device) is disposed at a level lower than the bottom surface of the interposer, it is considered to be “over” that surface (surface of the interposer substrate).” Office Action, page 5. It is respectfully submitted that the arrangement in Washida can be describes as non-coplanar, non-level, offset, below or above the surface of the substrate but the use of term, “over” is improper.

Claim 18 reads in part, “positioning a first semiconductor device over a first surface of the interposer, at least one bond pad of the first semiconductor device being exposed to the receptacle; positioning a second semiconductor device over a second surface of the interposer...”

Without limiting the scope of independent claim 18, and merely by way of example, the American Heritage Dictionary of the English Language, Fourth Edition (2000, Houghton-Mifflin Co.) defines the term “over” to mean “[i]n or at a position above or higher than” and “[a]bove the top or surface.”

Again, with respect to the subject matter to which independent claim 18 is drawn, Washida includes no express or inherent description of positioning first and second-level semiconductor devices over the surface of an interposer. The description of Washida is limited to positioning the first and second-level semiconductor devices “above the hole section 701a.” Col. 5, lines 6-9; Fig. 1. Further, the disclosure of Washida is limited to an assembly method that includes positioning “the second semiconductor device 760 [so that it] is lodged in the hole section 701a.” *Id.*

It is clear from the disclosure of Washida that that neither of the first or second level semiconductor devices laterally overlaps or is positioned over the interposer 701. No plan view figures that show relationship of the semiconductor elements and the interposer are provided. However, the specification continues to explain that “the lead terminals 707 of the first semiconductor device are connected to the respective lands 706 on the mounting substrate (interposer) 701, so that the first semiconductor device 750 is supported by the mounting substrate (interposer) 701 via the terminal leads 707 (Col. 5, lines 10-14). Thus, rather than

being positioned over the interposer 701, the first and second level semiconductor devices of Washida are positioned over a hole 701a formed through the interposer 701.

Furthermore, referring again to Fig. 1 of Washida, the second-level semiconductor device 760 is within the hole 701a and clearly not over any portion of the interposer 701.

As such, it is respectfully submitted that Washida does not anticipate each and every element of independent claim 18, as would be required to maintain the rejection under 35 U.S.C. § 102(b).

Each of claims 19-21 is allowable, among other reasons, for depending directly or indirectly from allowable claim 18.

Claim 21 is further allowable since Washida lacks any express or inherent description that solder balls or any other conductive structures may be secured to the bond pads of either semiconductor device after that semiconductor device has been positioned relative to an interposer.

Oka

Claims 18, 19, 21, and 22 stand rejected under 35 U.S.C. § 102(e) for reciting subject matter which is assertedly anticipated by the subject matter described in U.S. Patent 6,441,495 to Oka et al. (hereinafter “Oka”).

The description of Oka relates to processes for securing leads to semiconductor devices. One of these processes is tape-automated bonding (TAB), in which the leads that are carried by a polymeric film (tape) are electrically connected to bond pads of a semiconductor die. FIGs. 17 and 18 of Oka illustrate the TAB process, which is described more fully in columns 13 and 14 of Oka. Polymeric tape is not substantially rigid.

As currently amended, independent claim 18, in the relevant part recites, “[a] method for assembling semiconductor device components, comprising: providing an interposer with a substantially planar, *substantially rigid* substrate and a receptacle formed substantially through the substrate...”

Again, the polymeric tape disclosed by Oka is not substantially rigid. As such, Oka does not expressly or inherently describe each and every element of the method of amended

independent claim 18. Therefore, the method of amended independent claim 18 is, under 35 U.S.C. § 102(b), allowable over the subject matter described in Oka.

Claims 19, 21, and 22 are each allowable, among other reasons, for depending directly or indirectly from allowable claim 18.

Claim 22 is also allowable since Oka neither expressly nor inherently describes positioning a semiconductor device that includes a redistribution circuit. In fact, Oka lacks any mention of a semiconductor device with a redistribution circuit.

It is respectfully requested that the 35 U.S.C. § 102 rejections of claims 1-8 and 18-22 be withdrawn.

Rejections under 35 U.S.C. § 103(a)

Claims 1-6 and 9-17 stand rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

DiCaprio in View of Nishihara

Claims 1-6 and 9-12 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in U.S. Patent 6,452,278 to DiCaprio et al. (hereinafter "DiCaprio"), in view of teachings from U.S. Patent 6,469,395 to Nishihara et al. (hereinafter "Nishihara").

DiCaprio teaches an assembly process that includes positioning a first die 12 within an aperture 15 of a substrate 14, positioning a second die 50 over the first die 12, and electrically connecting the first and second dice 12 and 50 to conductors (metal layers 16) on the upper surface of the substrate 14. Figs. 3-4; col. 2 lines 24-58; col. 3, lines 26-46.

Nishihara teaches a method that includes positioning a first semiconductor chip 2a within an opening in a central portion of a first surrounding substrate 6a, electrically connecting the first semiconductor chip 2a to the first surrounding substrate 6a using wire bonding 5 or to a wiring substrate 1 using flip chip bonding, and placing a second semiconductor chip 2b on the first surrounding substrate 6a, superimposed over both the first surrounding substrate 6a and the first semiconductor chip 2a. Figs. 1-2; col 2, lines 30-69.

Claim 1, as currently amended, is directed to a method that includes "...electrically connecting . . . at least one first-level semiconductor device to . . . conductors on the upper surface of [a] substrate by first-level conductive members that are at least partially carried by [a] second-level semiconductor device..."

Both DiCaprio and Nishihara lack any teaching or suggestion of electrically connecting a first-level semiconductor device to "first-level conductive members that are at least partially carried by the second-level semiconductor device."

As such, it is respectfully submitted that the combination of teachings from DiCaprio with the teachings of Nishihara does not teach or suggest all the limitations of amended independent claim 1 and, thus, that the teachings of these references do not support a *prima facie* case of obviousness against amended independent claim 1. As such, the subject matter to which amended independent claim 1 is directed is, under 35 U.S.C. § 103(a), allowable over the teachings of DiCaprio and Nishihara.

Each of claims 2-6 and 9-12 is allowable, among other reasons, for depending directly or indirectly from allowable claim 1.

Urushima in View of Morinaga

Claims 13-14 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Urushima, in view of teachings from U.S. Patent Publication 2002/0047214 to Morinaga et al. (hereinafter “Morinaga”).

Claims 13-14 are each allowable, among other reasons, for depending either directly or indirectly from independent claim 1, which is allowable.

Urushima, Morinaga, and Taniguchi

Claims 15-17 have been rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is allegedly unpatentable over the teachings of Urushima, in view of teachings from Morinaga and, further, in view of the subject matter taught in U.S. Patent 6,388,333 to Taniguchi et al. (hereinafter “Taniguchi”).

Claims 15-17 are each allowable, among other reasons, for depending indirectly from independent claim 1, which is allowable.

DiCaprio, Nishihara, and Morinaga

Claims 13-14 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over teachings from DiCaprio, in view of the teachings of Nishihara and, further, in view of the subject matter taught in Morinaga.

Claims 13-14 are each allowable, among other reasons, for depending either directly or indirectly from independent claim 1, which is allowable.

DiCaprio, Nishihara, Morinaga, and Taniguchi

Claims 15-17 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in DiCaprio, in view of teachings from Nishihara and Morinaga and, further, in view of Taniguchi.

Claims 15-17 are each allowable, among other reasons, for depending indirectly from independent claim 1, which is allowable.

Entry of Amendments

It is respectfully requested that the proposed claim amendments be entered. The proposed amendments do not introduce new matter into the application, nor would they require an additional search. In the event that a decision is made not to enter the proposed claim amendments, entry thereof upon the filing of a Notice of Appeal in the above-referenced application is respectfully requested.

CONCLUSION

It is respectfully submitted that each of claims 1-22 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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